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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,802	11/25/2003	Alex Rabinovich	89160.0021	9760

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EXAMINER	
SHINGLETON, MICHAEL B	
ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 03/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,802	RABINOVICH ET AL.	
	Examiner	Art Unit	
	Michael B. Shingleton	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-15 and 22* is/are rejected.

7)☒ Claim(s) *9, 16-21, 23 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Michael B. Shingleton
MICHAEL B. SHINGLETON
PRIMARY EXAMINER
ART UNIT 2817

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1-12-2004 one sheet*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 12 and 14 are objected to because of the following informalities: In claim 12, "the gain and phase adjusting circuit" is recited. Claim 1 upon which claim 12 depends fails to recite a "gain and phase adjusting circuit". Thus it is clear that applicant meant "a gain and phase adjusting circuit instead. In claim 14 "the outermost" loop is claimed yet there appears to be no antecedent basis for this. Thus it is clear that "an outermost loop" was meant. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 7, 8 and 10-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshikawa et al. 5,691,668 (Yoshikawa).

Figures 3, 5 and 7 along with the relevant text of Yoshikawa discloses a dual loop feedforward power amplifier structure having an input like element 11 that is provided with a multi-carrier, i.e. multi-channel signal (See column 1, around line 5). Elements like 13, 19, 14, 20 and 15 form a first feedforward amplifier structure and elements like 6, 17, 18 and 21 form a second feedforward amplifier structure wherein the first feedforward power block serves as the main amplifier gain block in the second feedforward power amplifier. The first feedforward power amplifier structure contains a first error amplifier 20. The second feedforward amplifier block has a third and fourth loop as is clearly illustrated. These additional loops formed over a single feedforward amplifier is what corrects for what applicant calls "small signal distortions" thereby allowing the distortion cancellation to be more than 40 dB (See column 6, around line 21). The carrier cancellation loop of the first feedforward amplifier functions to extract an error signal representative of the error products produced by the main amplifier 19 and generates an output comprising an error signal representative of the distortion produced in a main amplifier (Note the couplers 13, 14, and 15.). As the first feedforward amplifier is utilized as the main amplifier of a second feedforward structure and elements 24 and 28 performs gain and phase adjustment, the function of canceling the multi-carrier signal present at the output of the first feedforward power amplifier is clearly present. Element 20 forms the error amplifier of the first error amplifier loop. Figure 5 of Yoshikawa shows the automatic gain control that is applied to the error amplifier via the attenuator 23. With respect to claim 5, the error amplifier 20 itself being a non-adjustable amplifier allows for

constant gain and phase characteristics of the dual loop feedforward power amplifier to be provided in the error amplifier 20. This constant gain and phase characteristics of the non-adjustable amplifier occurs with or without the monitoring of the output of the dual loop feedforward power amplifier.

With respect to claim 7 here it is recited that the first error amplifier loop functions independently of the other loops of the dual loop feedforward power amplifier. Because the output of the first feedforward amplifier is sensed the structure of Yoshikawa is capable of providing this function. In fact column 6 around line 40 of Yoshikawa clearly points out to the fact that the sensor 55 controls 23 and 27 of the error loop and 56 controls 25 and 29 of the second feedforward error loop.

With respect to claim 8 note that element 31 is part of the first path, and element 15 is a first injection coupler, elements 23 and 27 form gain and phase adjusting circuits in a second path and the error amplifier 20 forms a third path and element 54 forms a second injection coupler wherein "re-injection" occurs at the second injection coupler. Note that the output of the first injection coupler is connected to the second injection coupler.

With respect to claims like claim 10, the phase shifter 28 is a delay filter as it provides delay or phase shift. Therefore the output of the main amplifier module is coupled to this delay filter 28 through at least elements 19, 31 and the output is sampled as noted above via element 55.

With respect to claims like claim 11, the output of the first feedforward amplifier, that is sampled, is coupled to a second coupler 17 to generate a secondary signal which is applied to the delay line 33 as is clearly illustrated.

With respect to claims like claim 12, note that the carrier cancellation loop of the first feedforward amplifier has as path that includes an input signal at the output of the gain and phase adjusting circuit 24 and 28. This input signal is delayed by delay line 30 and it is this delayed copy of the input signal present at the output of the gain and phase adjusting circuits 24 and 28 that is subtracted from the attenuated copy of the main amplifier signal (Note that there will be an inherent attenuation by the element 53.) via the coupler 14 to thereby form a error signal "g".

With respect to claims like claim 13 the control 57 of Yoshikawa is the means by which the error amplifier 20 is "stabilized".

Note that with respect to claim 14 that the means for stabilizing an error amplifier 20 in Yoshikawa includes means for generating a pilot signal (Note element 51.), a delay line 31, "the outermost loop" can be met by the error cancellation loop of the first feedforward amplifier, a first error amplifier loop that includes a first coupler 14 and an error amplifier 20 wherein the first error amplifier

loop utilizes the pilot signal to stabilize gain and phase of the error amplifier (See column 6, around line 24).

With respect to claim 15, element 57 is the means for monitoring the error amplifier 20 performance by measuring spectral purity at the output of the error amplifier using a second coupler 55. This stabilizes the error amplifier. Within the element 57, the signal from the coupler 55 is applied and the signal from the pilot source 51 is applied. The pilot signal is then monitored, i.e. compared with that measured to "make the pilot signal component minimum" via the adjustment to gain and phase adjustment elements 23 and 27. Thus the phase and amplitude of the pilot tone at the input of the error amplifier 20 are compared to another phase and amplitude of the pilot tone at the output of the error amplifier via the coupler 55.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshikawa 5,691,668 (Yoshikawa).

As recited by column 6, around line 26 of Yoshikawa the distortion cancellation is more than 40 dB. However, Yoshikawa is silent on how much more than 40 dB the distortion cancellation is. The +40 dB is approximately 45 dB as set forth in claim 6 of the instant invention. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have selected optimized component values to be such that a 45 dB distortion is obtained, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable range involves only routine skill in the art. In re Aller, 105 USPQ 233.

With respect to claim 22, Yoshikawa is silent on the exact structure of the control circuit 57 that forms the means for comparing the phase and gain of the amplified pilot signal to the gain and phase of the input pilot signal. Claim 22 recites that this control circuit or "means for comparing phase and amplitude of the pilot tone" is a "processor". Processors are well known control components in a feedforward amplifier arrangement.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replaced the control unit of Yoshikawa with a processor because as the Yoshikawa reference is silent on the exact structure of the control unit one of ordinary skill in the art would have been motivated to use any art-recognized equivalent controller such as the processor. Note that one of ordinary skill in the art would have been further motivated to make the combination so as to allow for the programmability of the controller.

Allowable Subject Matter

Claim 9, 16-21, 23 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Rabinovich et al. 6,958,647 and Rabinovich et al. 6,946,906 are related to the instant application.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 and after July 15, 2005 the fax number will be 571-273-8300. Note that old fax number (703-872-9306) will be service until September 15, 2005.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
March 19, 2006

Michael B Shingleton
Primary Examiner
Group Art Unit 2817